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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,175	09/28/2000	Victor Konrad	042390.P9573	2921

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EXAMINER
ROSSOSHEK, YELENA

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,175	KONRAD ET AL.	
	Examiner	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-19 and 22-28* is/are rejected.

7)☒ Claim(s) *4,5,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ditlow et al. (US Patent 5,311,079).

As to claims 1 and 17 Ditlow et al. teaches determining an optimum splitting variable as input lines x_1, x_2 and x_3 input Boolean variables and y_1 and y_2 as output Boolean variables (col. 3, ll.44-46; ll.52-54; Fig. 9); dividing a set of equations representing a programmable logic array (PLA) into a first set of equations representing a first sub-PLA and a second set of equations representing a second sub-PLA based on splitting variables (Fig. 8); determining a topological circuit representation of the equations by presenting the Fig. 2 and Fig. 3 wherein the Fig. 2 represents a first sub-PLA and Fig. 3 represents a second sub-PLA (col. 4, ll.1-6); applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA as shown in the equations (col.5, ll.60-67; col. 6, ll.1-29; col. 8, ll.34-38); and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption using the

selective activation approach to activate the pullup devices (col. 2, ll.65-68; col. 3, ll.1-4; ll.8-12).

3. Claims 10, 12-14, 24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Katkoori et al. ("Simulation based architectural power estimation for PLA-based controllers ").

As to claims 10 and 24 Katkoori et al. teaches determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) by specifying the number of output variables (|O|), the number of input variables (|I|) and the number of terms (|T|) for synthesizing a PLA using a set of Boolean equations (Page 122); dividing the set of equations representing the PLA into equations representing a plurality of sub-PLAs as shown on the Fig. 1 representing the PLA block as a set of sub-components (Page 122); merging outputs of the equations representing the plurality of sub-PLAs as shown as a part of the fragment of VHDL code (Page 123); determining a topological circuit representation of the equations representing the plurality of sub-PLAs as shown on the Fig. 1; applying gating logic to the topological circuit representation of the plurality of sub-PLAs within a typical PLA which is implemented as AND-OR structure which is logic of gates; controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption within the modeling of power consumption due to node activity in AND plane and OR plane is more involved (Page 123).

As to claims 12-14 and 26 Katkoori et al. teaches the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting

variable for each equation representing a sub-PLA wherein the power characterization involves extracting equations for different sub-components of PLAs (abstract); each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA; a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs within the minimization of equations obtained after the logic minimization (Page 123).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 3, 6-9, 18, 19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ditlow et al. (US Patent 5,311,079) as applied to claim 1 above in view of Shau (US Patent 6,492,835).

As to claims 2, 3, 6-9, 18, 19, 22 and 23 Ditlow et al. teaches merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA as shown on the Fig. 9 which is represents the PLA/decoder and divided portion of it shown on the Fig. 2 and Fig. 3 (col. 4, ll.57-62);

the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented as shown on the Fig. 2 the output lines y_1 and y_2 and product terms lines PT1-PT4 are realized in the table on the Fig. 9 and the output lines (DD, TD, CD, CC, DC) as shown on the Fig. 3 can be activated according the input lines x_2 and x_3 (col. 4, ll.35-40); delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA (col. 2, ll.14-18); determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA as shown on the Fig. 10 (col. 6, 48-54). However Ditlow et al. lacks the specifics regarding computer aided design and the structure of OR plane in the PLA. Shau teaches the PLA to be divided is partially optimized by computer aided design (CAD) (col. 1, ll.20-25); an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA; an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA; determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design (abstract). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Shau to teach the specifics subject matter Ditlow et al. does not teach, because a

large PLA is divided into smaller sub-PLA while individual sub-PLA's are controlled separately which makes it possible to save power with better performance and better cost efficiency.

6. Claims 11 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katkoori et al. as applied to claims 10 and 24 above, and further in view of Shau.

As to claims 11 and 25 Katkoori et al. teaches the limitations from which the claims depend. However Katkoori et al. lacks specifics regarding computer aided design. Shau teaches the PLA to be divided is partially optimized by computer aided design (CAD) (col. 1, ll.20-25). It would have been obvious to one of ordinary skill on the art at the time the invention was made to have used Shau to teach the specifics subject matter Katkoori et al. does not teach, because a large PLA is divided into smaller sub-PLA while individual sub-PLA's are controlled separately which makes it possible to save power with better performance and better cost efficiency.

7. Claims 15, 16, 27 and 28 arte rejected under 35 U.S.C. 103(a) as being unpatentable over Katkoori et al. as applied to claims 10, 12, 24 and 26 above, and further in view of Ditlow et al.

As to claims 15, 16, 27 and 28 Katkoori et al. teaches the limitations from which the claims depend. However Katkoori et al. lacks specifics AND plane. Ditlow et al. teaches determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; selecting a column with smallest overhead in the AND plane of the equations representing the PLA as shown on the Fig. 10 (col. 6, 48-54). It would have been obvious to one of

ordinary skill on the art at the time the invention was made to have used Ditlow et al. to teach the specifics subject matter Katkoori et al. does not teach, because it makes possible to activate the pullup devices associated with the product terms selectively, based upon decoding and selective activation approach, which provides a significantly greater reduction in the power consumption.

Allowable Subject Matter

8. Claims 4, 5, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA; and the OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 703-305-3827. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HR

LEIGH M. GARBOWSKI
PRIMARY EXAMINER